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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/815,446	03/22/2001	Christopher A. Bode	2000.068000/TT4149	7640

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EXAMINER	
CRAIG, DWIN M	
ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/815,446	BODE ET AL.	
	Examiner	Art Unit	
	Dwin M. Craig	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-33 have been presented for reconsideration based on Applicants' Request for Continued Examination Under 37 CFR § 1.114 and amended claim language and arguments. Claim 34 has been presented for Examination.

Response to Arguments

2. Applicants' arguments presented in the 4-20-2005 responses have been fully considered. The Examiner's response is as follows.

2.1 As regards Applicant's response to the 35 USC § 112 first paragraph rejections the Applicants' argued, *on page 16 of the 4-20-2005 response,*

Although Applicants respectfully disagree with this contention and respectfully assert that the term "predetermined amount of residual error" is indeed enabled from the disclosure relating to the comparison of the predetermined threshold tolerance compared to the residual error, disclosed on page 14, line 24-page 15, line 6 of the specifications.

The Examiner notes that the claimed limitation of a predetermined amount of residual error is defined in Applicants' specification to mean a *predetermined threshold tolerance.* This predetermined tolerance is interpreted to mean a value of merit discovered from past measurements acquired during the process of fabrication of semi-conductor wafers. An artisan of ordinary skill in the wafer fabrication art would have been able to collect measurement data from past fabrication production runs and then have been able to calculate a *threshold tolerance* with out undue experimentation, for this reason the 35 USC § 112 rejections are withdrawn.

2.2 As regards the Applicants' response to the 35 USC § 102 rejections of the claims.

Applicants' argued, *on page 18 of the 4-20-2005 responses,*

Conrad does not disclose determining a field mean error as called for in claim 1 (as amended). Even though Conrad discloses residual errors, a field mean error is not calculated.

The Examiner notes that on page 14 are the following, *the field-mean error data corresponds to the average overlay error relating to a particular field from one process to another.* The Examiner has found Applicants' argument to be persuasive and withdraws the 35 USC § 102 rejections of the claims.

2.3 An updated search has revealed new art.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-34 are rejected under 35 USC § 102(b) as being anticipated by **US Patent 5,877,861 Ausschnitt et al.**

3.1 As regards Independent Claims 1, 11, 15, 16, 26 and 29 and using independent Claim 1 as an example, the *Ausschnitt et al.* reference discloses,

processing at least one semiconductor device (Figure 12 item 80 EXPOSED WAFER),

acquiring metrology data from said processed semiconductor device; (Abstract),

performing a field-to-field metrology analysis based upon said metrology data to determine a field-mean error; (Col. 2 line 40, The field term alignment errors are calculated from the within-level between-field overlay measurement using the processor. The Examiner notes that field term alignment errors are the same as field-mean error.),

determining a wafer-mean error; (ABSTRACT, Simultaneous use of between-field overlay metrology to control field term alignment error at al levels and *level-to-level* metrology to control file term, and translational alignment errors at all levels is applied. The Examiner notes that Level-to-level metrology is the same as wafer-mean error metrology analysis.),

comparing said field-mean error to said wafer-mean error; (Col. 2 line 42, The correction factors are calculated from the field term alignment errors and the level-to-level overlay measurements using the processor.),

performing residual-error analysis based upon said field-to-field analysis and said wafer-mean error, said residual-error analysis comprising determining whether significant residual error exists as a result of comparing said residual error with a predetermined tolerance, said residual-error being based upon said comparison of said wafer-mean error and said field-mean error data; and (Col. 1 line 20, A requirement of the manufacturing process is to keep the alignment error, between levels, below acceptable product *tolerances*. And Col. 6 line 39, The equations are solved using any technique such as "least squares" best fit or any other mathematical technique for solving for the unknown variables based on minimization of the *residual* error.),

performing at least one of a field-level adjustment and a wafer-level adjustment based upon said residual-error analysis. (Col. 2 line 44, the field layers are then aligned based on the correction factors.).

3.2 As regards dependent **Claims 2, 12-14, 17, 28, 32, 33** the *Ausschnitt et al.* reference discloses, processing said semiconductor device in a subsequent manufacturing process based

upon said residual-error analysis (Col. 6 line 42, The calculated terms are fed back to the lithography tool to correct overlay errors...).

3.3 As regards dependent **Claims 3, 18, 27 and 30** the *Ausschnitt et al.* reference discloses wafers (Figure 12 item 80).

3.4 As regards dependent **Claims 4, 19 and 34** the *Ausschnitt et al.* reference discloses field-to-field metrology data analysis (Col. 2 line 37, Next, the level-to-level field and within-level between-field errors are measured using overlay targets and metrology equipment.).

3.5 As regards dependent **Claims 5-10, 20-25 and 31** are all directed towards determining alignment and overlay errors and programming a machine to compensate for these errors. The *Ausschnitt et al.* reference discloses determining alignment errors (Figures 1A-1E. 2A-2C), field errors (Figures 3A-3B, 4, 5, 6), fixing alignment (Figure 7), and programming a machine to calculate and compensate for these measured errors (Summary of the invention Col. 2 lines 30-48).

Conclusion

4. **Claims 1-34** have been presented for reconsideration and Examination. Claims 1-34 have been rejected. This Office Action is **Non-Final.**

4.1 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M. Craig whose telephone number is (571) 272-3710. The examiner can normally be reached on 10:00 - 6:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo P. Picard can be reached on (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMC

Paul L. Rodriguez 7/22/05

Primary Examiner
Art Unit 2125